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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/816,926	ARNOLD ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1. Claims 1-25 have been examined.

Papers Received

2. Receipt is acknowledged the amendment papers, where the papers have been placed of record in the file.

3. The objections to the title, specification, and claims, as well as the 35 USC 112 rejections have been overcome by the amendment and are herein withdrawn.

Information Disclosure Statement

4. The information disclosure statement filed 9/10/03 failed to comply with 37 CFR 1.98(a)(3) because it did not include a concise explanation of the relevance, as it was presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that was not in the English language. It had been placed in the application file, but the information of documents J, K, and L referred to therein had not been considered. See MPEP (A) (3).

5. If the Applicant wishes for the German Documents to be considered on their independent merits, a new information disclosure document for those documents must be submitted along with a concise explanation of relevance. As stated in MPEP 609 (C) (1) regarding faulty information disclosure statements, "Applicant may then file a new information disclosure statement or correct the deficiency in the previously filed IDS, but the date that the new IDS or correction is filed will be the date of the IDS for purposes of determining compliance with the requirements based on the time of filing of the IDS (37 CFR 1.97)."

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-11, 16-22, and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Baxter (5,794,062).

8. In regard to claim 1, Baxter discloses a configurable hardware block (figure 4 and column 9, lines 22-24) comprising: a universal configurable unit being selectively configured to read data stored in a memory unit, to process the data in at least one of arithmetic and logical processing units, and to write data representing a result of the processing to the memory unit, said universal configurable unit having an asynchronous combinational circuit to asynchronously link components of said universal configurable unit, and said universal configurable unit being capable of interacting autonomously with external hardware. [Column 24, lines 52-59 show that an ALU/shifter receives data from RAM (random access memory) and performs arithmetic and logical operations on the data, where the result is written back to RAM. Figure 4 shows that the configurable hardware block receives and sends external signals on transmission lines 40, 42, 44, 46, and 48 and thus interacts with some external hardware. As shown in figure 1 and column 10, lines 36-39 show that the GPIM (General Purpose Interconnect Matrix -

element 16) is used to transfer data between S-machines (configurable hardware block (column 10, lines 33-34)) or link the S-machine components. Column 11, lines 24-29 show that the S-machines each have their own independent clock rates relative to any other S-machine. This means that in order for the GPIM to facilitate communication, it must be an asynchronous circuit because there is no coherence is clock signals. Figure 16 shows the structural makeup of the GPIM (column 10, lines 1-3) and there is no indication of any sort of synchronous control that links all the data of lines 380 and 382. Column 10, lines 39-45 along with figure 1 show that each S-machine is capable of interacting with external hardware. This interaction is autonomous since each S-machine performs such interaction independent from every other S-machine. This would be further facilitated with the above cited section showing that each S-unit has independent timing and thus each act independently in communication with external devices. Thus a universal configurable unit is disclosed as called for in claim 1.]

9. In regard to claim 2, Baxter discloses the configurable hardware block according to claim 1, wherein the hardware block is configured for interaction with the external hardware comprising instructing the memory unit to accept data supplied by the external hardware in response to specific events. [Figures 9A and 9B show that transmission line 46 is connected to memory. Column 24, lines 56-58 show that data from this external-memory is routed to the RAM (memory) units and thus the RAM memory is instructed to accept data from the external hardware. Since this data transfer is selectively routed as shown in the section, the inherent control signal of a specified value making this selection is the specific event that the transfer is in response to.]

10. In regard to claim 3, Baxter discloses the configurable hardware block according to claim 1, wherein the hardware block is configured for interaction with the external hardware comprising outputting one of data and signals to the external hardware. [As shown in figure 4 signals are output from the hardware block to an external memory and other external hardware on transmission lines 46 and 48.]

11. In regard to claim 4, Baxter discloses the configurable hardware block according to claim 1, wherein the external hardware is selected from the group consisting of other configurable hardware blocks, a control unit operating in parallel or at a supervisory level, and other components of a system containing the configurable hardware block. [Transmission line 46 is shown to be the medium for interaction with an external memory (an I/O device) in figures 4, 9A, and 9B, and transmission line 48 is shown in figure 2 to be used for interaction with a T-Machine, both of which are components of the system (figure 1) containing the configurable hardware block.]

12. In regard to claim 5, Baxter discloses the configurable hardware block according to claim 4, wherein the data and/or signals output to the external hardware are used to signal specific states or events. [Figure 4, shows that the external signals on line 48 are control signals and thus inherently control some sort of event or occurrence.]

13. In regard to claim 6, Baxter discloses the configurable hardware block according to claim 1, which comprises a timer generation unit generating a clock signal for the memory unit. [Figure 9B shows that each register of the memory unit 192 has a clock input fed by line 70, which is generated by the IFU (instruction fetch unit). Since this unit generates the clock (timer) signal, one can call it a timer generation unit.]

14. In regard to claim 7, Baxter discloses the configurable hardware block according to claim 6, wherein said timer generation unit is configured to generate the clock signal depending on one or more periodic or non-periodic signals originating at least to some extent from the external hardware. [Figure 5 shows that line 70 is from an instruction state sequencer. The figure also shows that this sequencer depends on a signal (40) from an external local time-base unit. Column 11, lines 3-7 show that this signal is a clock signal and thus a periodic or non-periodic signal from external hardware.]

15. In regard to claim 8, Baxter discloses the configurable hardware block according to claim 1, which comprises a signaling unit configured to generate report signals for the external hardware. [Applicant has defined report signals, on page 22 of the specification, to be signals that indicate one or more states or events. Figure 4 illustrates several report signal transmission lines for the external hardware. Lines 42, 44, 46, and 48 all output control signals to the external hardware. Subsequently, each of these signals is inherently used for some purpose and thus they indicate some sort of event (that has happened or is to be triggered) and are report signals. Since these signals are sent by each unit shown in figure 4, the entire configurable hardware block is the signaling unit.]

16. In regard to claim 9, Baxter discloses the configurable hardware block according to claim 8, wherein the report signals signal an occurrence of predefined states and/or events in the configurable hardware block. [As shown in column 24, lines 56-61, data is to be written to an external memory and thus an indication of this event must be sent on

line 46 (figures 9A and 9B) as an I/O signal to the memory so that this external hardware receives the data properly.]

17. In regard to claim 10, Baxter discloses the configurable hardware block according to claim 8, wherein said signaling unit is configured to generate a report signal signaling that an operation or sequence of operations to be executed repeatedly in the hardware block has been executed a specified number of times. [Column 12, lines 14-17 show that a directive is set at the beginning and end of an inner-loop portion (code sequence; column 11, lines 53-56) that indicates that the sequence has been completed one time. Lines 24-28 then show that this directive causes a reconfiguration of hardware. Figure 17 shows that in the event a reconfiguration is required (step 1010), multiple steps are performed including generating transition control signals (step 1004). This is done by the signaling unit, which has been shown to be the configurable hardware block above, as shown in column 37, lines 24-43, where the IFU portion handles this functionality. Since the inner-loop portion has completed, a signal signifying this event must be sent to memory so that a new set of instructions is obtained.]

18. In regard to claim 11, Baxter discloses the configurable hardware block according to claim 8, wherein the signaling unit is configured to generate a report signal useable as an interrupt request for a program-controlled unit. [Column 37, lines 44-57 show that upon an interrupt request, the system is reconfigured. With an interrupt to service and a new hardware configuration a new program state and execution must be

initialized as shown in figure 17 steps 1006 and 1008. This means new program instructions must be retrieved from memory using a report signal indicating this event.]

19. In regard to claim 16, Baxter discloses the configurable hardware block according to claim 1, which comprises a plurality of configurable units selected from the group consisting of sub-units selectively configurable to a required function, configurable data paths, and configurable signal paths. [As shown above, the design shown in figure is the configurable hardware block. It is shown that this block comprises a plurality of units, which are also configurable since the units together are configurable. Column 12, lines 24-32, show that the different configurations specify instruction formats, opcodes, data formats, addressing modes, etc. Therefore, different configurations of all these elements are used. This means that different sizes of operands and instructions due to these formats exist and thus the widths of the signal paths, which lead to the external memory (as shown above) for retrieval of such information, are configurable.]

20. In regard to claim 17, Baxter discloses the configurable hardware block according to claim 16, wherein configurable data and signal paths to the external hardware exist or can be established (as shown above).

21. In regard to claim 18, Baxter discloses the configurable hardware block according to claim 1, wherein the memory unit is a register block containing a plurality of registers. [Column 24, lines 41-42 show that the RAM memory comprises registers.]

22. In regard to claim 19, Baxter discloses the configurable hardware block according to claim 1, configurable on a basis of instructions or instruction sequences,

and configurable to execute operations or operation sequences specified by the instructions or instruction sequences. [Column 12, lines 24-32 shows that each configuration is based on different ISAs (instruction set architectures) and thus based on the instructions that execute on that ISA. Since these ISAs are the basis for the hardware configurations, the processor is configured to execute operations specified by the instructions of that ISA.]

23. In regard to claim 20, Baxter discloses the configurable hardware block according to claim 19, dimensioned to be configurable by hyperblock. [Applicant has defined in the specification a hyperblock to be a block of like-code that is handled together. As shown in figure 3A, code sequences of like instructions (instructions of the same ISA) are shown to be executed together before the hardware is reconfigured to handle another of these blocks of code.]

24. In regard to claim 21, Baxter discloses the configurable hardware block according to claim 1, constructed and configurable to be used to replace a specific circuit. [Column 12, lines 24-29 show that each configuration is implemented and optimized for use of a particular ISA. This means that each configuration is configurable to replace a specific fixed circuit with the same functionality for the same ISA.]

25. In regard to claim 22, Baxter discloses the configurable hardware block according to claim 1, constructed and configurable to be used to replace various specific circuits. [Column 12, lines 24-29 show that each configuration is implemented and optimized for use of a particular ISA. This means that the configurations are

configurable to replace various specific fixed circuits with the same functionality for the same ISAs.]

26. In regard to claim 24, Baxter discloses the configurable hardware block according to claim 21, wherein the hardware block is configurable for use in applications selected from the group consisting of cryptography and identification applications. [Column 11, lines 66-67, shows that a pattern searching application may run on the system. A pattern searching program searches for and identifies a certain pattern and is thus an identification application.]

27. In regard to claim 25, Baxter discloses the configurable hardware block according to claim 1, which comprises a memory unit for storing interim results. [The RAM units shown above are shown in column 24, lines 41-42 to provide temporary or interim storage for data. Lines 58-59 show that results are stored in these RAMs as well and therefore there exists a memory unit for storing interim results.]

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baxter in view of Rupp (5,784,636).

30. In regard to claim 12,

a. Baxter discloses the configurable hardware block according to claim 8. Baxter also discloses the use of image processing and compression techniques in column 11, lines 62-67.

b. Baxter does not disclose the hardware block comprising at least one comparison unit generating and outputting a report signal.

c. Rupp discloses a reconfigurable computing system (column 1, lines 6-11) comprising at least one comparison unit generating and outputting a report signal. Column 46, lines 9-15, show that comparing is done (and thus a comparison unit is used) for video compression. Lines 30-49 show the steps involved in this compression and specifically lines 30-33 show that a comparison is the basis for whether further processing is performed or not. For further processing, more instructions are inherently needed to perform these operations and if no further processing is needed, no more instructions for these operations are needed and other programming ensues. This would cause a report signal, based on this event, to signify to the external memory which instructions to fetch when implemented in the design of Baxter.

d. This ability to compress video data into a smaller format would have motivated one of ordinary skill in the art to modify the design of Baxter to use the video encoding scheme that includes the comparison unit taught by Rupp.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Baxter to include the video encoding scheme that includes

comparison units as taught by Rupp so that video compression can be used to compress video data and thus save space.

31. In regard to claim 13, Baxter in view of Rupp discloses the configurable hardware block according to claim 12, wherein at least some of said comparison units are configurable comparison units configured to subject incoming signals to operations selected from the group consisting of selectable compare operations, checks for TRUE, and checks for UNTRUE. Column 46, lines 30-33 of Rupp show that a data signal is checked to see if it is below (or smaller than) a threshold (another data signal). This is a selectable compare operation as the term is defined in claim 14.

32. In regard to claim 14, Baxter in view of Rupp discloses the configurable hardware block according to claim 13, wherein the selectable compare operations are selected from the group of compare operations consisting of greater than, greater than or equal to, not equal to, smaller than, and smaller than or equal to comparisons as shown above.

33. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baxter in view of Rupp as applied to claims 12-14 above, and further in view of Hennessy.

34. In regard to claim 15,

a. Baxter in view of Rupp discloses the configurable hardware block according to claim 12,

b. Baxter in view of Rupp does not explicitly disclose wherein at least some of said comparison units have a multiplexer connected in series on an input side

thereof, said multiplexer determining which signals are supplied to said comparison unit as input signals.

c. Baxter in view of Rupp does show in column 46, lines 30-31 that each new macro block is compared with a current estimated macro block. Thus, the disclosure inherently includes some sort of selection hardware so that each data block can be selected at the appropriate time for comparing in the comparison unit. Hennessy shows on page 351 that a multiplexer is synonymous with the term data selector, which is exactly what the function of Baxter in view of Rupp is performing. Page B-9 of Hennessy shows the simple design of a multiplexer.

d. This simple design would have motivated one of ordinary skill in the art to modify the design of Baxter in view Rupp to make the disclosed selection hardware a multiplexer as taught by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Baxter in view of Rupp to use the multiplexer disclosed by Hennessy as the data selection hardware so that a simple selection hardware design may be realized.

35. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baxter in view of DeHon.

36. In regard to claim 23,

a. Baxter discloses the configurable hardware block according to claim 21,

b. Baxter does not disclose that the hardware block is configured to test an integrated circuit containing the hardware block.

c. DeHon has shown on page 23 that monitoring and debugging of a reconfigurable logic system takes place. Applicant states that monitoring and debugging are different than testing and provides reference to an area of the specification. The Examiner asserts that this section of the specification does not precisely indicate a definition of "test" but merely gives examples of tests. Further, there is no definition for the terms "monitor" or "debug". The included dictionary definition of "debug" as it pertains to computer science shows that to debug is "to search for and correct malfunctioning elements or error in". The definition of "test" shows that testing simply involves determining properties of something. Therefore, a debug process, which searches for errors (a property) is also a test process. That said, since the reconfigurable circuit is contained in an integrated circuit, the integrated circuit is being tested when the reconfigurable circuit is being tested.

d. One of ordinary skill in the art would have recognized that the use of the testing design given by DeHon would advantageously allow the integrated circuit that contains the reconfigurable hardware block to not be flawed and not allow untended errors to occur.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Baxter to use the testing given by DeHon so that the integrated circuit is shown to not be flawed and so untended errors do not occur.

Response to Arguments

37. Applicant's arguments filed 10/19/04 have been fully considered but they are not persuasive.

38. Applicant has argued that neither Baxter, Rupp, DeHon, nor Hennessy asynchronously link the S-machines (components of the universal configurable unit) nor does Baxter disclose these devices interacting autonomously with external hardware as recited in claim 1. As shown in figure 1 and column 10, lines 36-39 show that the GPIM (General Purpose Interconnect Matrix - element 16) is used to transfer data between S-machines (configurable hardware block (column 10, lines 33-34)) or link the S-machine components. Column 11, lines 24-29 show that the S-machines each have their own independent clock rates relative to any other S-machine. This means that in order for the GPIM to facilitate communication, it must be an asynchronous circuit because there is no coherence is clock signals. Figure 16 shows the structural makeup of the GPIM (column 10, lines 1-3) and there is no indication of any sort of synchronous control that links all the data of lines 380 and 382. Column 10, lines 39-45 along with figure 1 show that each S-machine is capable of interacting with external hardware. This interaction is autonomous since each S-machine performs such interaction independent from every other S-machine. This would be further facilitated with the above cited section showing that each S-unit has independent timing and thus each act independently in communication with external devices. Thus a universal configurable unit is disclosed as called for in claim 1.

39. Applicant has argued that though the DeHon reference facilitates for the reconfigurable hardware to be monitored and debugged, it does not provide an

indication that the reconfigurable hardware may be configured to test an integrated circuit as recited in claim 23. Applicant also states that monitoring and debugging are different than testing and provides reference to an area of the specification. The Examiner asserts that this section of the specification does not precisely indicate a definition of "test" but merely gives examples of tests. Further, there is no definition for the terms "monitor" or "debug". The included dictionary definition of "debug" as it pertains to computer science shows that to debug is "to search for and correct malfunctioning elements or error in". The definition of "test" shows that testing simply involves determining properties of something. Therefore, a debug process, which searches for errors (a property) is also a test process. That said, since the reconfigurable circuit is contained in an integrated circuit, the integrated circuit is being tested when the reconfigurable circuit is being tested.

Conclusion

40. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

41. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl

Examiner
Art Unit 2183

SFG
December 22, 2004

RICHARD L. ELLIS
PRIMARY EXAMINER